Nanosecond Peak Detect and Hold Circuit with Adjustable Dynamic Range

Gabriel Fellner, Lucas Speckbacher, Seyed Mostafa Mousavi, David Johannes Pommerenke, Satyajeet Shinde, Michael Hillstrom, Ram Chundru and Cheung-Wei Lam

***Abstract*— This paper presents a novel peak detect and hold (PDH) circuit for the measurement of the peak voltage of electromagnetic-field probes. These probes are used to capture the fields generated by electrostatic discharge (ESD) events in non-grounded portable devices. Therefore, a circuit combining small size, low power consumption and nano-second operation is needed. A topology using a discrete bipolar transistor structure with OTA and common-base storage capacitor charge control optimally meets the requirements. The circuit performance is demonstrated for different bias point settings. The error between the captured value and the actual pulse peak value is shown as a function of rise time, pulse length, amplitude and bias settings. A comparison with literature, shows unmatched performance with respect to speed and power consumption. Using the bias settings the PDH circuit can be adjusted to the sensor's frequency response to minimize power consumption in a multi-channel system containing sensors of different bandwidth.**

***Index Terms*— Amplitude estimation, Analog circuits, Bipolar transistor circuits, Electromagnetic compatibility, Electromagnetic fields, Pulse measurements, Signal detection**

I. INTRODUCTION

TYPICAL applications requiring the use of PDH-circuits are measurement systems where a sensor generates a narrow pulse, for example in spectrometers using semiconductor-detectors and where the information is in the signals peak value. Numerous papers have been published on these applications in nuclear radiation spectroscopy [1], x-ray spectroscopy [2] and optical spectroscopy [3], [4]. In these applications, the output signal from the detector is a train of narrow current pulses which is converted to a voltage signal by a charge sensitive amplifier (CSA) or transimpedance amplifier (TIA) and then fed to a PDH which enables analog to digital conversion with low sampling-rate. In the field of electromagnetic compatibility (EMC), test methods with pulses in the lower nano-second range are also used such as ESD- and TLP-testing [5]–[8].

This paper presents a PDH circuit used for electromagnetic field probes, capturing the fields during ESD events on non-grounded devices using a cigarette pack size, battery powered sensor system. Several electromagnetic D-dot and B-dot field sensors, all optimized for different frequency bands are used for transient field analysis. The sensors use partial self-integration to adjust the pulse response. The ESD severity information we are interested in is captured by the peak value of the sensor response. This covers the frequency range of interest of different ESD events.

The fastest expected rise time from the sensors in our application is 0.5 ns and the shortest pulse width to be detected is 2 ns. A peak detection method is required for this parameter range, along with the ability to integrate the system into a mobile test platform, which requires low power consumption and small form factor. Such a sensor system has been introduced as a mobile platform in [9], details of the implemented probes are explained in [10].

Multiple options exist for capturing nanosecond pulses. Fast A/D converters, such as those used in oscilloscopes capture the complete pulse. However their size, power consumption and data processing requirements are not suitable for this application, where only peak detection is required. A peak detect and hold (PDH) circuit forms a cost effective solution with small form factor, that enables to realize multiple channels in portable size and battery powered operation.

The most important parameters for characterization of PDH circuits are:

- Amplitude accuracy
- Dependency on pulse shape, minimum detectable pulse-width
- Dynamic-Range
- Hold-time
- Power consumption
- Size

The PDH circuit presented in this work, has unmatched speed compared to published circuits from literature. This superior performance is shown using a measurement setup allowing characterization of analog PDH circuits regarding the key parameters of the input signal. Characterization of the circuit for different operating points shows, that adjusting the speed/power trade-off allows the reduction of power

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consumption for sensors with lower bandwidth. The paper uses material from the thesis [11] with permission.

II. Proposed PDH

An overview on existing analog and digital PDH circuits for nanosecond pulses was already reported in [12]–[14]. There are five basic topologies for analog peak detect and hold circuits as shown in Fig. 1.

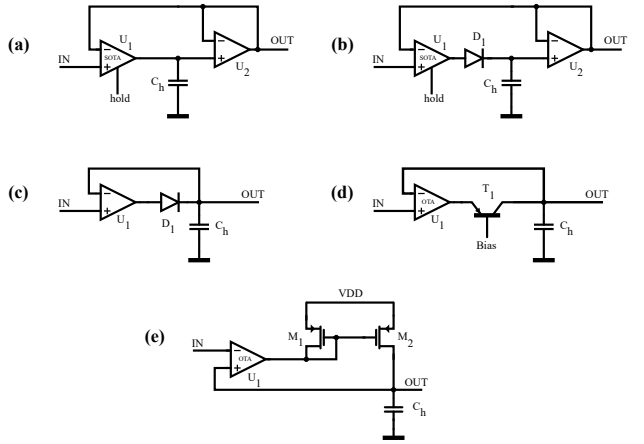

Fig. 1 Peak detect and hold topologies

A. Triggered Track and Hold

Circuits using track and hold structures (Fig. 1 (a)) require a trigger signal which changes the operation from the track- to hold-phase when the input peak voltage is reached. The generation of this can be challenging for fast pulses, because the timing of the trigger event has strong impact on the performance of the circuit. Most common methods for the generation of these trigger signals are *leading edge discrimination* and *constant fraction discrimination* [23], whereas the first strongly depends on the pulse shape [3].

B. Triggered Track and Hold with Diode Capacitor Configuration

A sampling transconductance amplifier (SOTA) in combination with a diode capacitor combination (Fig. 1 (b)) reduces the effect of trigger timing because the charging current of the hold capacitor is rectified by the diode. With the ability of changing the SOTA operation from track to hold operation, the reverse leakage current through the diode is reduced after a peak has been detected. Since a diode is used in the circuit the disadvantages of its nonlinear behavior and dynamic on-resistance arise [4].

C. Diode Capacitor Configuration with Amplifier

At a diode-capacitor configuration with amplifier (Fig. 1 (c)) the amplifier is in voltage follower configuration and the diode rectifies the charging current. By supplying the amplifier feedback voltage with the voltage at the hold capacitor the diode drop is eliminated. For amplifiers with low input impedance a voltage buffer is required to provide the feedback voltage. This topology is very common due to its simplicity and good performance. The disadvantages are the nonlinear behavior of the diode, leakage current and cross-talk through the diode's parasitic capacitance [13]–[16].

D. Common-Base Configuration with an Amplifier

A pnp-transistor in common-base configuration with a hold capacitor supported by an amplifier (Fig. 1 (d)), offers many advantages over using a diode. The main advantage is the current gain which reduces the voltage swing requirement of the amplifier output and the adjustable bias voltage at the base which allows suitable adjustment of the operating point of the amplifier. There are still drawbacks such as nonlinear behavior, reverse leakage current and cross-talk through the base-emitter capacitance [2], [17]–[19].

E. OTA with a Current Mirror

The use of an OTA and current mirror for rectification (Fig. 1 (e)) instead of a diode is common in integrated circuit technology. The OTA behaves as a voltage dependent current source, where the current is equal to the charging current of the hold capacitor. The topology especially benefits from the simple implementation in a CMOS process and the low cross-talk through the gate-drain capacitance. A major concern is given by the fact that even after a peak voltage has been detected current is flowing through the current-mirror. This current flow continues until the output voltage of the OTA reaches a voltage, high enough to turn the transistor M_1 completely off. Since very high-speed designs use a small value hold capacitor and a current-mirror with large transconductance this effect increases significantly [1], [20]–[22].

III. Proposed PDH

A. Concept

The concept of the proposed circuit is shown in Fig. 2. In addition, its full schematic without a discharge switch (JFET) is depicted in Fig. 3. Fig. 4 shows a picture of the circuit with a size of about 20 x 15 mm.

The circuit consists of an OTA with clamping network at the output, followed by a pnp-transistor in common-base configuration. This transistor allows charging the hold capacitor by providing low input impedance to the OTA output and blocks the discharge of the hold capacitor by its high output impedance. The voltage used for the feedback of the OTA cannot be directly supplied by the node of the hold capacitor because of the high base current of the input differential pair transistor. An impedance converter is needed. A high-speed voltage buffer consisting of a n-channel JFET and a npn-transistor is introduced providing low input bias current. The JFET provides low input bias current and transconductance, while the npn-transistor provides current gain for driving capacitive loads.

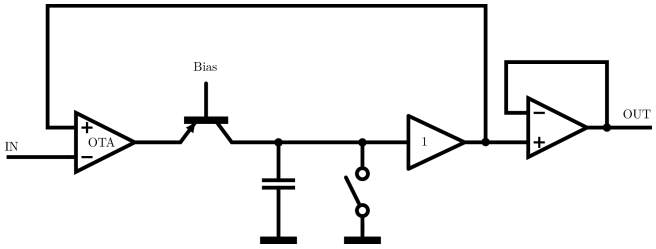

Fig. 2 Basic building blocks of the proposed PDH circuit concept.

The bias point of the circuit is controlled by a micro controller unit (MCU) using DACs and ADCs. Circuit parameters such as tail bias current, feedback bias current and common-base bias voltage can be controlled.

Compared to the already published circuits using the concept of an OTA combined with a transistor in common base circuit and hold capacitor [17]–[19], this circuit is optimized for nano-second peak detection. This was achieved by linearization of the OTA transfer characteristic and software adjustable bias points. By software adjustment the dynamic range / speed of the circuit can be adjusted for the required operation and also temperature drift of the bias point can be compensated. This enables matching the requirements of each channel to the expected signal, especially in multi-channel PDH systems. Considering a PDH-system which is connected to different electromagnetic field sensors, and where the field sensors have different bandwidths, the PDH-circuit can be matched to the requirement of the sensor to achieve maximum power efficiency.

B. Operational Transconductance Amplifier

RF-bipolar transistors are used for achieving high bandwidth of the OTA. In the amplifier, the input differential pair (T_1, T_2) is loaded by a pnp-current-mirror (T_4, T_5) for differential to single-ended conversion. A current sink consisting of a npn-transistor (T_7) was used as the tail current bias, whereby the value of the bias current can be adjusted by changing the base voltage of this transistor using a DAC. The current is measured by reading the voltage drop across the emitter degeneration resistor (R_4) using the ADC.

The transistors of the input differential pair (T_1, T_2) use a small value emitter degeneration resistors (R_e). These resistors provide a small negative feedback and extend the amplifiers linear operating region to approximately $R_e I_e$. This extension of the linear region is especially important for reducing the rise-time dependency of the circuit. The internal rise-time of the voltage across the hold capacitor is thereby reduced making feedback delay less critical. The clamping of the output voltage is done using a Schottky diode (D_1) with a series resistor (R_d) connected between diode connected pnp-transistor of the current mirror load and the output of the amplifier. During the peak detection phase this diode is reverse biased. After a peak is detected and the circuit changes to the hold phase, the clamping network starts conducting and supplies half of the tail current, resulting in a minimum output voltage of:

$$V_{OTA\,min} = V_{DD} - V_{EB} - V_{clamp} \tag{1}$$

where V_{EB} is the Emitter-Base voltage of the pnp-current-mirror load and V_{clamp} is the voltage drop of the clamping network, with:

$$V_{clamp} = \frac{I_{tail}}{2} R_d + V_{diode} \tag{2}$$

This clamping of the output voltage reduces the effect of the cross-talk through the rectifying pnp-transistors (T_6) collector-emitter capacitance. The error generated by this cross-talk is defined by:

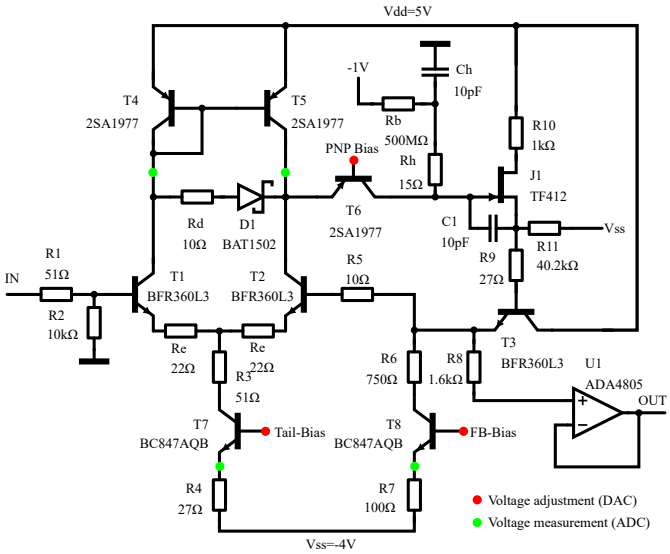

Fig. 3 The proposed PDH circuit schematic, JFET as discharge switch not shown.

$$V_{error} = \Delta V_{OTA} \frac{C_{CE}}{C_{CE} + C_h} \tag{3}$$

Where ΔV_{OTA} is the voltage swing at the emitter of the rectifying pnp-transistor.

The diode series resistor in the clamping network is required to damp oscillations that may be caused by the parasitic inductance of the clamping diode. When a pulse is detected and the circuit changes its operation to hold phase (condition: $V_{in} < V_{Chold}$), the current through the clamping network rises very fast. The node at the cathode of the diode is a high impedance node during this phase, as it is connected to the collector of T_5 and T_2, and T_6 is reverse biased. This combined with the fast current rise through the diode this can cause oscillations since the parasitic inductance of the diode and the capacitance at the high ohmic node can form an LC-circuit with positive feedback through the PNP-current mirror. A series resistor was added for damping this LC-circuit.

To ensure that the clamping network is reverse biased, the voltage across the clamping network is also measured.

C. Common-Base Rectifier

The transistor in common-base configuration (T_6) is used for rectification. Due to the low input impedance provided by the current gain the required voltage swing of the amplifier is reduced. The most important parameters which effect the operation of the circuit are the current gain and the parasitic capacitances. The emitter-base capacitance leads to a small negative feedback because when the emitter voltage increases the base voltage also increases, while the collector-emitter capacitance discharges the hold capacitor when the emitter voltage decreases, producing an voltage error as described above.

By adjusting the bias voltage at the base the output voltage of the OTA can be changed and set to a value so that the clamping network is reverse biased with 50 mV, enabling the best performance for the amplifier.

D. Voltage Buffer

The voltage buffer has a constant offset voltage, which is defined by:

$$V_{offset} = V_{GS} + V_{BE} \quad (4)$$

Where V_{GS} is the gate-source voltage of the n-channel JFET (J_1) and V_{BE} the base-emitter voltage of the NPN-transistor (T_3), the voltage drop across the series resistor is neglected. Due to the fact that the JFET has negative gate-source voltage the offset cancels out to a certain extent depending on the used bias currents and components.

Since the feedback of the amplifier is in reference to the output voltage of the buffer this offset does not affect the output voltage of the PDH, but remains across the hold capacitor.

It is very important that the voltage buffer has a flat frequency response in the working range. Deviations from this flat response result in output signals that are either too large or too small depending on the input pulse frequency content. To achieve this flat frequency response even at higher frequencies, a speed up capacitor (C_1) is added between the gate and the drain of the JFET.

E. Limitations

The presented circuit has limitations, which can be influenced by certain design parameters. The response to very short pulses is limited by the ability of the circuit to transfer charge to the hold capacitor (C_h). The transferred charge is determined by the current and the time this current is present at the hold capacitor. For low amplitudes the corresponding absolute value of the output current of the OTA is low, because of the finite transconductance. For low output currents, a significant portion of the output current is used to charge the output capacitance of the OTA, to enable current flow through transistor (T_6). Therefor more time (larger pulse-width) is required to reach a desired voltage level at the hold capacitor.

The maximum output current of the OTA is limited by the OTA tail current. This leads to limited charge transfer to the hold capacitor if the pulse-width is very short.

A general limitation for the maximum input voltage amplitude comes from the value of the positive supply voltage. This value defines the bias voltage of the common base circuit of transistor (T_6) to approximately the base voltage of the current mirror pair (T_4, T_5). This limits the maximum voltage at the hold capacitor to the base voltage of T_6, since above this voltage level the collector-base diode gets conductive.

F. Important Design Aspects

Designing a PDH circuit for a time range in the lower nano second range can be very challenging because of the many trade-offs to be dealt with, such as an oscillations tendency and respond speed. The following aspects are crucial for optimizing the speed of the circuit and avoiding oscillations:

- Small and compact structures keeping time delay low
- Bias current sources should be decoupled with resistors as close as possible to the RF-part and with values as high as possible in order to minimize reflections.
- Minimize parasitic capacitances and inductances
- In simulation consider the expected feedback delay, including physical path length
- Avoid the use of multiple components within one package in bias or feedback transistors if they lengthen the routing and as they increase cross coupling

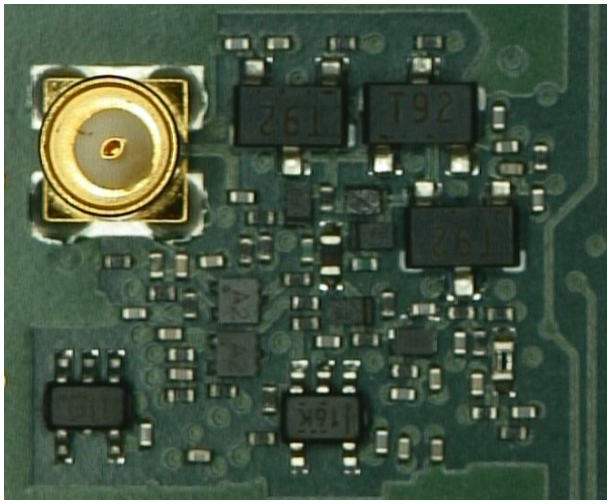

Fig. 4 PCB of PDH circuit with dimensions of 20 mm x 15 mm.

IV. Measurement Setup

The circuit is characterized on its behavior for different rise- and fall-times, amplitudes and pulse-widths. Fig. 5 shows a block diagram of this measurement system comprising an arbitrary waveform generator (Tektronix AWG7102 with 10 GS/s) for pulse generation. Two programmable step-attenuators (Peregrine PE43702 and Minicircuits DAT-15R5A+) and an Amplifier Research 10W power amplifier (10W1000AM3) are used to adjust the pulse amplitude. Overall 24 dB attenuators are used to set the amplitude range to the region of interest. The step attenuators have a range of 15.5 dB and 31.75 dB. By combining the step attenuators with a reduction of the amplitude at the AWG (6 dB), a dynamic range of more than 53 dB is achieved. By reducing the amplitude at the AWG further, even a higher dynamic range is possible. Amplitude reduction is preferably done with step-attenuators to maintain high signal to noise ratio (SNR) as the AWG suffers from a rather high background noise. At the DUT (PDH) the input voltage peak and the output voltage are measured with a Rhode & Schwarz 4 GHz, 20 GSa/s oscilloscope (RTO2044). During the measurements the adjustment of the circuit operating point is done by sending commands from the control PC to the MCU.

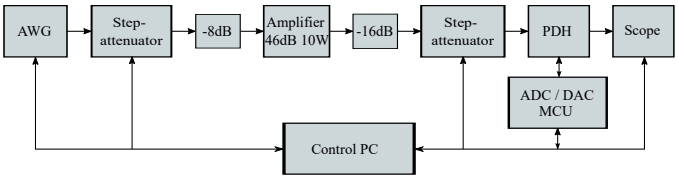

Fig. 5 Block-diagram of the measurement setup

Using this measurement setup, the key parameters of analog PDH circuits can be analyzed for three core characteristics along the amplitude of the pulse: hold-behavior, dependency on pulse rise-time and dependency on pulse-width.

V. Measurement Results

A. Analysis of the Hold-Behavior

An input pulse with a rise- and fall-time of 4 ns and a pulse-width of 10 ns was used for an initial characterization of the hold-behavior of the circuit. With this relatively slow rise-time and large pulse-width, information about the basic circuit operation is gained. The droop-rate of the circuit is determined by sampling the PDH response after different time intervals. Fig. 6 shows the measurement error after different sampling times, an overshoot of up to 12 % is observed. The output voltages sampled after 200 ns are higher than the input peak voltage but for sampling after 1 µs the result is very close to the ideal value. Also the voltage droops somewhat from 1 µs to 5 µs. The reason for this is that there is a small transient peak in the first few 100 ns, which disappears after about 500 ns. The reason for this is the speedup capacitor at the voltage buffer which pushes the voltage level to high and then slowly discharges with the bias current of the JFET.

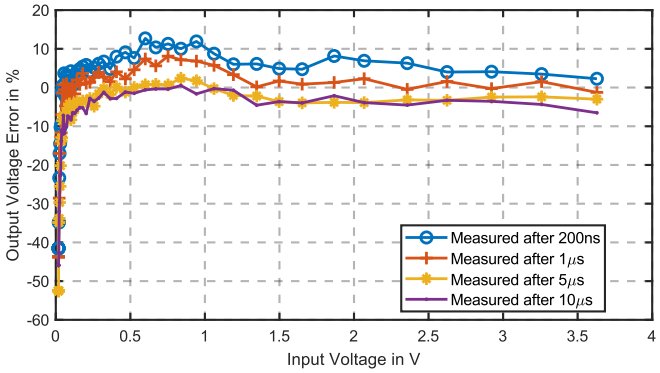

Fig. 6 Output error observed during the hold behavior measured for different time periods after the input pulse. The output voltage error is calculated using the input peak voltage as a reference. The circuit operating point was set with a tail current of 15 mA

B. Analysis of Rise-Time Dependency

To analyze the impact of the input signal rise-time the PDH is tested using pulses with different rise-times but long pulse-width of 10 ns. The use of a slow waveform ensures that the circuit can perform its basic operation, so that the effect of the different rise-times only affects the output signal. During this measurement the output voltage was measured 100 ns after the input pulse. In Fig. 7 the error of the output voltage is shown across the whole input voltage range. It shows a maximum rise-time dependency of 10 %, which is a reasonable number in this range of rise-times and for the expected application of capturing fields of ESD. The dependency on rise-time of about 10 % is already close to the limitations of the test setup, because a certain proportion of the error is caused by the amplifier in the test system. At fast rise-times this amplifier causes a small amount of overshoot in the range of a few percent, which results in some measurement error for the input peak voltage that is used for the error calculation.

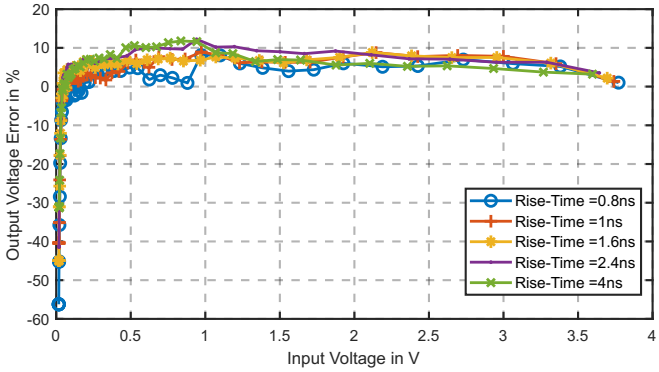

Fig. 7 Output error measurement result showing the rise time dependency, measured after 100 ns. The circuit operating point was set with a tail current of 15 mA and a feedback bias current of 1.5 mA.

C. Analysis of Pulse-Width Dependency

In order to specify the dependency on the pulse-width, a pulse with 800 ps rise- and fall-time was used, which enables testing down to pulse-widths as small as 1.5 ns. Again the value for the output voltage was taken after 100 ns. Fig. 8 shows that the output voltage is too low for smaller pulse-widths in the upper input voltage range. This is a result of limited charging current and limited time for the hold capacitor.

A very similar behavior can be obtained from Fig. 9 for the lower input voltage range, where the charging current for the hold capacitor is limited because of the small input differential voltage and limited transconductance of the OTA.

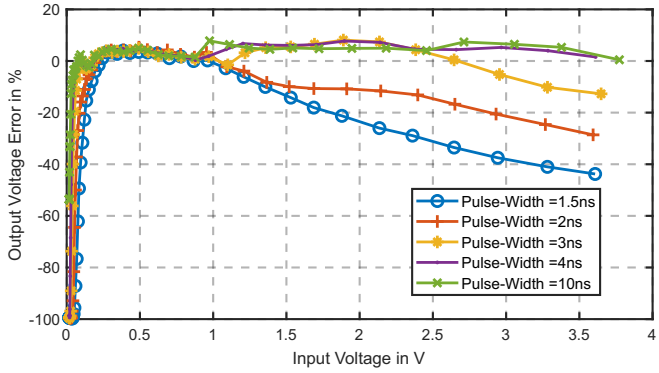

Fig. 8 Output error measurement results showing the pulse-width dependency for full input voltage range, measured after 100 ns. The circuit operating point was set with a tail current of 15 mA and a feedback bias current of 1.5 mA.

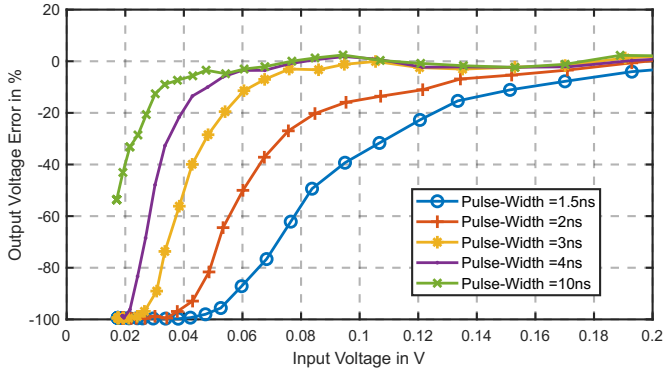

Fig. 9 Output error measurement result showing the pulse-width dependency for the lower voltage region, measured after 100 ns. The circuit operating point was set with a tail current of 15 mA and a feedback bias current of 1.5 mA.

D. Tail Current Adjustment

Changing the tail bias current of the OTA has the greatest effect on the circuit performance, because it directly effects the transconductance and the maximum output current. The circuit behavior was characterized for different values of this current, since the OTA tail bias current also makes a major contribution to the circuit power consumption.

In Fig. 10 and Fig. 11 the measurement results are shown for different values of the bias current, tested with a pulse-width of 3 ns and the output voltage again being sampled after 100 ns. First when looking at Fig. 11 it can be seen that the bias current mainly determines the behavior in the upper voltage region and the lower voltage region is much less affected.

The resulting dynamic range for different tail bias currents and pulse widths is shown in Fig. 12. It is clearly visible, that a change in the bias current causes the highest variation in the output voltage at the smallest pulse-width of 1.5 ns. The larger the pulse-width becomes, the less the tail bias current is required by the OTA for reaching large output voltages. As a result the necessary tail bias current can be set to a value, which fulfills the dynamic range requirements by using as little bias current as necessary and therefor providing high power efficiency.

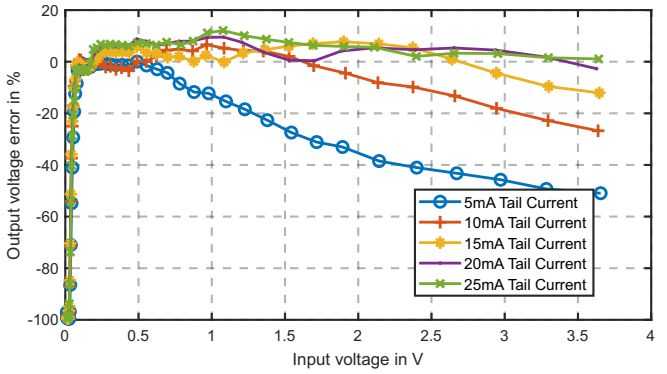

Fig. 10 Output error results for different tail bias current using a pulse-width of 3 ns, measured after 100 ns. The circuit operating point was set with a feedback bias current of 1.5 mA.

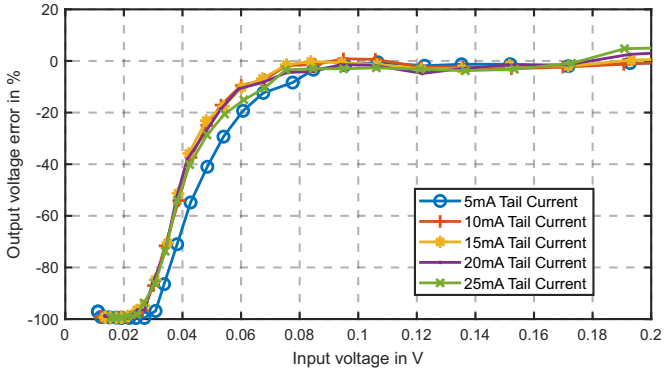

Fig. 11 Output error measurement result for different tail bias currents using a pulse-width of 3 ns in the lower voltage range, measured after 100 ns. The circuit operating point was set with a feedback bias current of 1.5 mA.

E. Characterization Results Summary

All the measurement results provide a good overview of the important circuit parameters and describe the influence of different bias points very well. In Fig. 12 the dynamic-range versus tail bias current is shown for the measured pulse-widths. The result shows, that the dynamic range for very short pulses can be increased significantly by increasing the bias current. Whereas for the 10 ns long pulse the dynamic range is lowered with a higher bias current, this is the case because the higher tail current leads to a higher voltage drop at the output of the OTA caused by the higher current through the clamping network.

For the calculation of the dynamic range a 3 dB deviation to the ideal output voltage was chosen for the lower- and upper-voltage-limits. In the event that there was no 3 dB deviation for the higher voltage levels 3.5 V was selected as the maximum voltage. It should be possible to operate the circuit with voltages up to 4 V, but this was not tested because the scope of this work focuses on very fast pulses and lower power consumption. For pulse-widths greater than 2 ns the measurement was only up to 3.5 V and therefore shows a lower dynamic range than is possible.

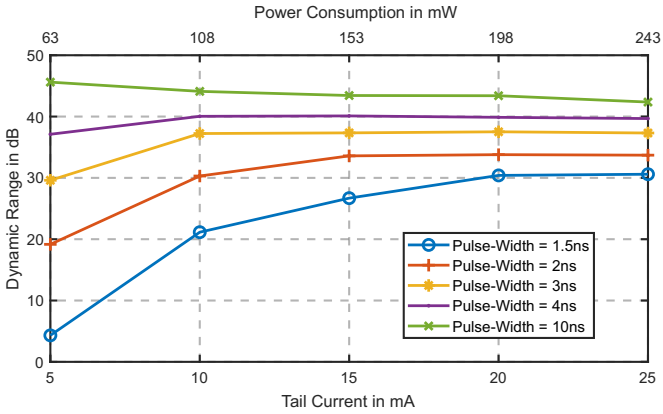

Fig. 12 Measurement result of the dynamic-range for different pulse-widths, measured after 100 ns. The circuit operating point was set with a feedback bias current of 1.5 mA.

F. Measurement with H-Field Sensor

Since the pulses in the application of measuring electromagnetic fields during ESD events show more complex waveshapes, the response of the circuit to a signal from a magnetic field sensor is tested. For this purpose a magnetic field probe (B-dot, 5 mm x 20 mm) is connected to the circuit and a human skin ESD event (4 kV) is triggered in a distance of 5 cm to the sensor. The corresponding sensor signal and response of the circuit is shown in Fig. 13.

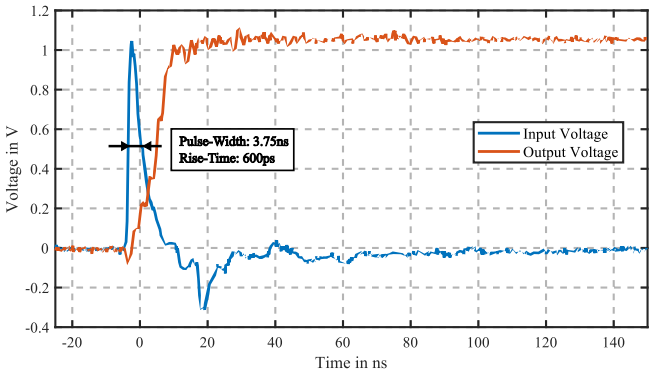

Fig. 13 Circuit response to signal of a magnetic field sensor located in a distance of 5 cm to 4 kV human skin ESD event. The sensor signal has a rise time of 600 ps and a pulse width of 3.75 ns.

VI. Performance Comparison

In Table I the existing published circuits are compared for the parameters that are relevant in this work. The comparison shows that the proposed circuit offers a much better minimum detectable pulse-width than the existing circuits, with a very low power consumption and good dynamic range. It needs to be noted that the authors of these publications often had different optimization goals, such as accuracy or linearity.

VII. Conclusion

A peak detect and hold circuit for nano-second pulses was designed and verified across different bias point settings. The measurement results reveal superior performance regarding speed and power consumption compared to results from literature. The use of different operating points maximizes energy efficiency by matching the circuit performance to the requirements of each specific's sensor response. Actively using this tradeoff between power and speed offers major advantages in battery powered multichannel systems, where multiple signals with different bandwidths have to be measured using similar circuitry. With the proposed PDH, pulses having a width of 3 ns can be detected with a dynamic range of 37 dB at a power consumption of only 108 mW and a dynamic range of 26.7 dB is achieved for pulse-widths of 1.5 ns at a power consumption of 153 mW.

TABLE I
PDH Performance Comparison

Topology	Min. PW	DR	Power	Design goal
Triggered track and hold [3]	20 ns	25 dB	N/A	speed
Triggered track and hold [4]	200 ns	N/A	120 mW	low-cost
Diode capacitor configuration with amplifier [15]	10 ns	50 dB	1.2 W	speed, precision
Common-base configuration with amplifier [17]	10 ns	N/A	N/A	speed, precision
Common-base configuration with amplifier [18]	N/A	46 dB	N/A	speed
Common-base configuration with amplifier [2]	N/A	N/A	N/A	precision
OTA with current mirror [20]	500 ns	N/A	200 µW	efficiency, CMOS IC
OTA with current mirror [1]	N/A	20 dB	N/A	precision
OTA with current Mirror [22]	200 ns	20 dB	6.6 mW	precision
Proposed circuit	1.5 ns	26.7 dB	108 mW	speed, efficiency
	1.5 ns	30 dB	198 mW	
	3 ns	37.23 dB	108 mW	

PDH performance comparison, PW: pulse-width, DR: dynamic-range, power: power consumption

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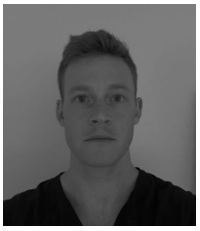

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